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THE MAGAZINE FOR COMPUTER APPLICATIONS

Circuit Cellar Online offers articles illustrating creative solutions and unique applications through complete projects, practical tutorials, and useful design techniques.

RESOURCE LINKS

A Guide to online information about:

Joint Test Action Group (JTAG) IEEE 1149.1 and IEEE 1149.4

by Bob Paddock

In issue 104, March 1999 of Circuit Cellar, Jeff Bachiochi wrote --- *Working with CoolPLD* --- where he touched upon the Joint Test Action Group (JTAG) interface, while covering the Philips CoolRunner PLD's. I had an application where I thought the CoolPLD's would be of use, and at the same time I wanted to learn more about the applications of JTAG myself, so I thought I'd share what I learned along the way.

First off, Xilinx has completed the acquisition of the CoolRunner line of low power CPLDs from Philips Semiconductors.

Xilinx continues to support the XPLA Professional design entry and implementation software tools for the CoolRunner CPLDs. They have also made the software available at no cost after registration. It can be downloaded from the Xilinx web site at http://www.xilinx.com/products/software/webpowered.htm.

The writers of the CoolRunner documentation had a sense of humor that lightens the mood of reading through stodgy documentation footnotes like: "Important Notice to Purchasers: the entire physical

universe, including this product, may one day collapse back into an infinitesimally small space. Should another universe subsequently re-emerge, the existence of this product in that universe cannot be guaranteed". Perhaps referring to Everett's 'Many Worlds' or Dr. Bohm's Hidden Variables of Quantum Mechanics. Alas, I wander off into one of those other 'Many Worlds' at times, the relevant point here being it seems that Xilinx's data will probably be less humorous since they have even removed the web site page on how to power the CoolRunners from grapefruit and other plant power sources.

Keeping with the theme of this Resource Page, Xilinx has an excellent Glossary on Boundary Scan/JTAG that would be a good starting point for anyone new to JTAG.

To get started with using JTAG devices, you need a simple program that can toggle the appropriate pins on a I/O port. Phillips had a program that allowed you to connect a series of JTAG devices to your parallel printer port. Xilinx has expanded on the program to allow it to automatically detect what type of cable you are using. It supports the Phillips Hypercable, the Xilinx Parallel Cable, and the Altera ByteBlaster Cable. The XPLA PC-ISP software can graphically display a JTAG chain, supporting up to 60 devices, from a mixture of manufacturers.

Warning: There are several places in the Philips documentation that incorrectly identify the pinout of the download cable. According to CoolRunner tech support, the correct cable is shown in the XPLA PC-ISP "Help" file. Note that it is a bottom view so you must use the mirror image of this for correct PCB layout pin numbering. I'm sure this has gotten a few people, it almost got me.

Xilinx has their own Boundary Scan/JTAG: Getting Started paper to check out.

With time-to-market more important than ever in the high technology marketplace, companies that can produce quality products with a short product development cycle-time have a competitive advantage. Designing testability into a system can play an important role in introducing a new high-technology product. A product that is 6 months late to market will only make 66% of the available profit compared to the 100% profit that it would have made had it been shipped on time. Product testing is a large part of shipping a quality product. It is something that should be considered at the very start of a design. It should not be seen as some nuisance paperwork that needs to be written before the Quality Control department lets you ship your new product out the door.

If you're not familiar with JTAG already you might be wondering how it fits in the product testing scheme of things. JTAG is a simple four-wire serial interface system for testing the interconnections between compliant components without having to resort to expensive equipment like a Flying Prober or X-Ray equipment.

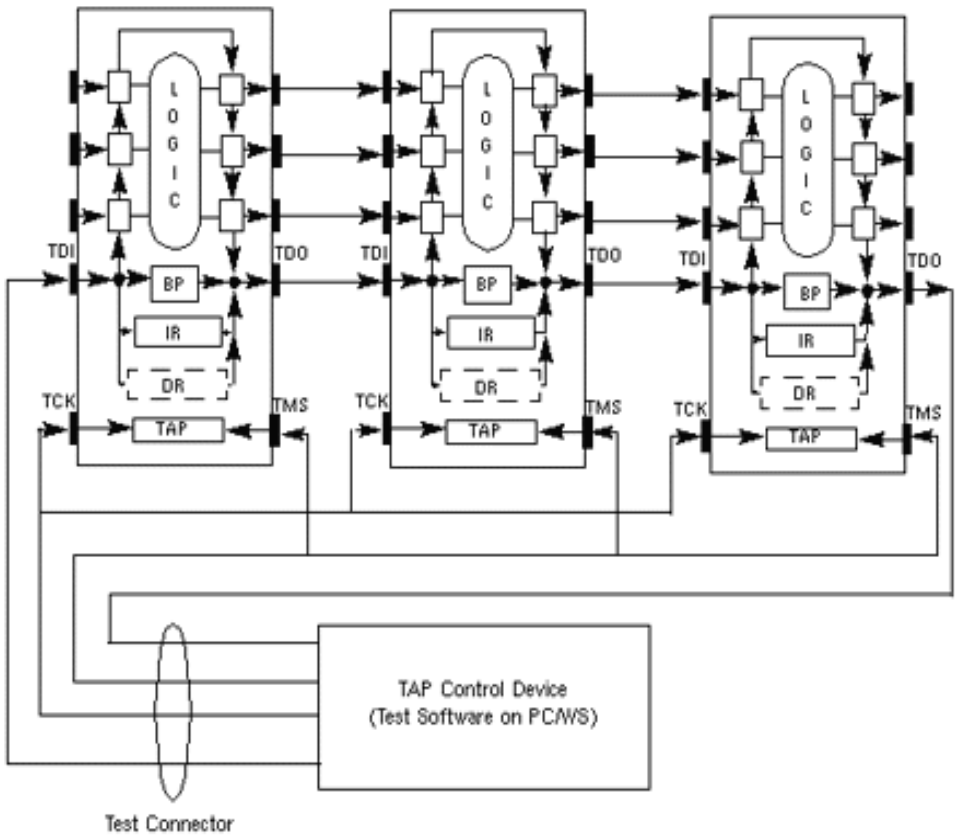
With newer package types, such as Ball-Grid Arrays, circuit testing is becoming more problematic. After all, how do you test something that has no pins and no access to the connections once the part is placed

on a board? You could use a socket, but that adds to the cost and eliminates some of the advantages of moving to the BGA package in the first place. Altera covers more about this in their paper Ball-Grid Array: An Ideal Package Option.

IEEE Std 1149.1 allows test instructions and data to be serially loaded into a device and enables the subsequent test results to be serially read out. Every IEEE Std 1149.1-compatible device has four additional pins—two for control and one each for input and output serial test data. To be compatible, a component must have certain basic test features, but IEEE Std 1149.1 allows designers to add test features to meet their own unique requirements. The specification was adopted as an IEEE standard in February 1990.

Since the JTAG port pins are already there, they have been pressed into service for such things as Flash memory programming and background debuggers. See *Taking Advantage of On-Chip Debugging Mechanisms* for more on background debugging.

Shown below is how a chain of three JTAG compatible devices would be hooked up. This graphic is taken from *Introduction to JTAG Boundary Scan* which is also available in PDF format as wpr-0018-01.pdf (10pp, 147KB). It gives the short and sweet overview of JTAG. It is part of Sun MICROELECTRONICS White paper collection.



A more detailed introduction can be found in Section two of Chapter fourteen of Application-Specific Integrated Circuits (ASICs... the book) by Michael John Sebastian Smith published by Addison-Wesley. It covers Boundary-Scan Testing and background in details. The book

can be found online at http://www.dacafe.com/Book/.

Almost all of the JTAG-related web pages I came across indicate that Texas Instruments JTAG information should be considered the mother lode of JTAG information. For example the Texas Instruments IEEE 1149.1 (JTAG) Testability Primer (ssya002c.pdf, 562.7 KB) can be downloaded as a single document. They even give JTAG its own homepage. Another useful page at TI is Educational Products.

The best way to see how all this might be useful is with a virtual hands-on WebCam. Intellitech offers a free evaluation version of their Eclipse software to learn about JTAG and IEEE 1149.1. Users will learn more about Intellitech JTAG debuggers and the IEEE 1149.1 (JTAG) standard. With JTAG software, a user is able to connect to an Eclipse Server via the Internet and perform JTAG diagnostic testing on a Texas Instruments JTAG/1149.1 Demonstration Board. The JTAG Demonstration Cam is a web camera focused on the Demonstration Board. The JTAG camera allows you to see the responses of the UUT (the demonstration board) via LED displays. You will need to enable JavaScript to see the Web Camera.

Many of the papers and links refer to boundary-scan description language (BSDL) files, you can see such a file for the Motorola MCF5202.

Some application notes from various manufactures show what and how the JTAG port can can be used beyond its intended purpose:

From Altera: *ISP via an Embedded Processor.*

From Cypress: *In-System Reprogrammable (ISR®) FAQ.*

From Intel are:

Designing for On-Board Programming Using the IEEE 1149 (JTAG) [.pdf].

Tips for Prototyping Using Today's Faster Embedded Processors.

Daisy Chaining: Connecting JTAG devices.

[If you have a large quantity of JTAG devices, then the TMI and TCK

lines should be independently buffered every few devices to prevent excessive loading of the lines.]

AP-630 Designing for On-Board Programming Using the IEEE 1149.1 (JTAG) Access Port. This document provides information on an alternative method for small form factor PCB applications. This document explains how you can use the IEEE 1149.1 (JTAG) Access Port to program Intel flash memories. This onboard programming method is ideal for space-constrained printed circuit board environments since you only need access to four land-pads to perform programming functions.

AP-720 Programming Flash Memory through the Intel386 EX Embedded Microprocessor JTAG Port. This application note describes a simple method for programming data into flash memory in the Intel386 EX embedded processor; however, the scope of this application is easily extended to many other JTAG compliant devices. Using the features of the Intel386 EX embedded processor in conjunction with a simple hardware interface, a standard set of software routines can be used to program data into flash memory. By controlling the CPU's JTAG port, these routines manage the data that is programmed into flash memory as well as the processors control lines.

Intel386 EX Processor JTAG Programming of Flash - Code.

Intel386 EX Processor Programming Flash Memory through the JTAG Port.

From Motorola: *Application Note AN1264 Application Note JTAG Flash Memory Programmer.* The download speeds possible using JTAG may prohibit its practicality for downloading the complete system software, but certainly it is ideally suited to download a small boot loader program into flash memory to control the remainder of the system download. Another key application area the technique supports are field upgrades where new software releases are loaded onto an existing customer system.

National's portfolio of SCAN test products lowers a system's cost of ownership over the course of its life cycle. SCAN products enable faster manufacturing, board tests, system check outs, and in-field diagnostics and repair.

The low power of SCAN CMOS Test Access Logic makes it ideal to surround non-JTAG-compliant devices for board-level test.

The SCAN PSC100F enables the use of a microprocessor to create an onboard embedded Test Master, freeing up external test equipment.

SCANPSC110F enables simultaneous testing of like boards as well as partitioning of complex systems. Use it on each board in a multi-drop or hierarchical system design. The advantage of a hierarchical approach over a single serial scan chain is improved test throughput and the ability to remove a board from the system and retain test access to the remaining modules.

The NASA ASIC Guide: Assuring ASICS for Space Draft 0.6 Published by Jet Propulsion Laboratory California Institute of Technology and National Aeronautics and Space Administration (the URL http://jpl.nasa.gov also has some interesting links)

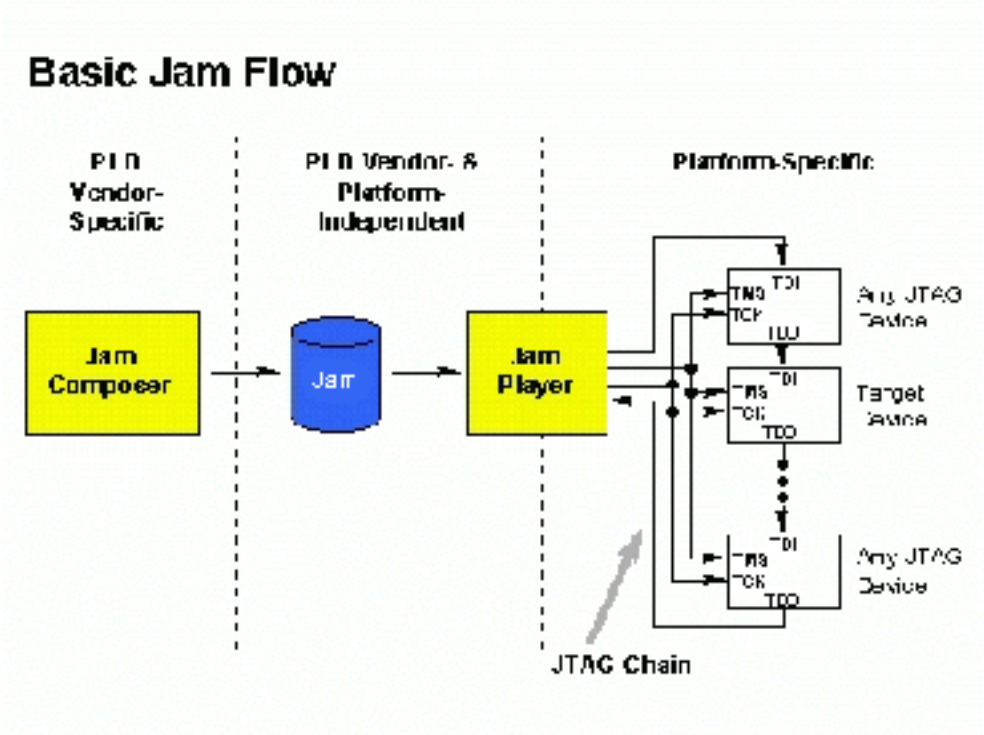
The NASA ASIC Guide draws from a broad range of ASIC experience. The JPL team called upon ASIC experts from the commercial world, academia, and numerous government agencies committed to high reliability microelectronics. A number of these experts agreed to sit on the NASA ASIC review board. The authors of the guide visited those in the field, such as NASA contractors and ASIC vendor customer support engineers, drawing from their experience. Combining the knowledge gained from the experts with the practical experience gained on the Cassini project, JPL developed the guide. Throughout the process, members of the NASA review board offered informed opinions as they critiqued the entire document.

JPL developed this guide to help NASA and NASA contractor communities obtain high-quality ASICs. The guide focuses on high reliability space applications, which frequently require radiation hardening to the natural space radiation environment. The authors provide a broad look at all the tasks involved in ASIC management and engineering, assuming sound managerial and engineering judgment prevails when actually implementing the details of your ASIC program.

The relevant section to our JTAG project here can be found in Chapter Two: Resource Planning. The entire guide is worth reviewing for the points on planning and managing a project.

ASIC TEST IT'S A NEW BALL GAME By Dan Strassberg is also worth a look.

The Jam programming language is compatible with PLDs that offer ISP. The Jam language is a major step forward in providing a software-level standard for in-system programming. Programming support for the Jam language is offered by an ever-growing number of vendors.



What is Jam?

The Jam programming and test language is a new standard file format for in-system programmability (ISP) purposes. The Jam language is designed to support programming or configuration of programmable devices and testing of electronic systems, using the IEEE 1149.1 Joint Test Action Group (JTAG) interface. The Jam language is a freely licensable open standard.

The Jam language was created by Altera engineers and is supported by a consortium of PLD manufacturers, programming equipment makers, and test equipment manufacturers. The consortium is proposing that the Jam language be adopted as an industry standard.

The Jam language addresses the issues designers face when programming PLDs in-system. These issues include proprietary file formats, vendor-specific programming algorithms, large file sizes, and long programming times. The Jam language is a major step forward in providing a software-level standard for in-system programming.

How the Jam Language Works can be found on Altera's site.

Complete Jam Language Specification (PDF) can be found on the Jam Home Page.

Software is a key component of boundary-scan testing and development for calculating the interconnection matrices to be tested. The following are a few of the related links:

JTAG [Joint Test Action Group], in 'Inside JTAG' [sidebar] (T. Coomes, A. Fritsch, & R. Tatge), in "Tools for Embedded-Systems Debugging" (C. Perez), Mar93, page 56 Dr. Dobb's Journal.

BSGEN, VHDL/BSDL Code Generator for DOS.

RSN Technology's Personal JTAG Download is a program for testing and debugging boards with JTAG ports.

JTAG was originally developed to test boards that couldn't be tested conventionally. As such, it comes from a high-end background, and both the hardware and software can be pretty expensive. Of course, that doesn't mean it isn't worth it, but it can be prohibitive for small companies or independent designers.

Personal JTAG is a tool for accessing the JTAG functions of a board via a simple low-cost parallel-port interface that you may already have. It includes a generic parallel-port driver that can be configured for different LPT-to-TAP mappings, and has presets for Altera's ByteBlaster and Lattice's ispDownload cables.

Corelis offers an extensive line of boundary-scan related software packages that share common architectures and can be used in conjunction with all Corelis' hardware platforms. Boundary-scan software is available for Windows 95, Windows 98, and Windows NT. ScanPlus JTAG Test Software.

Corelis Inc., Unveils A High-Performance PCMCIA Boundary-Scan (JTAG) Test Controller Board.

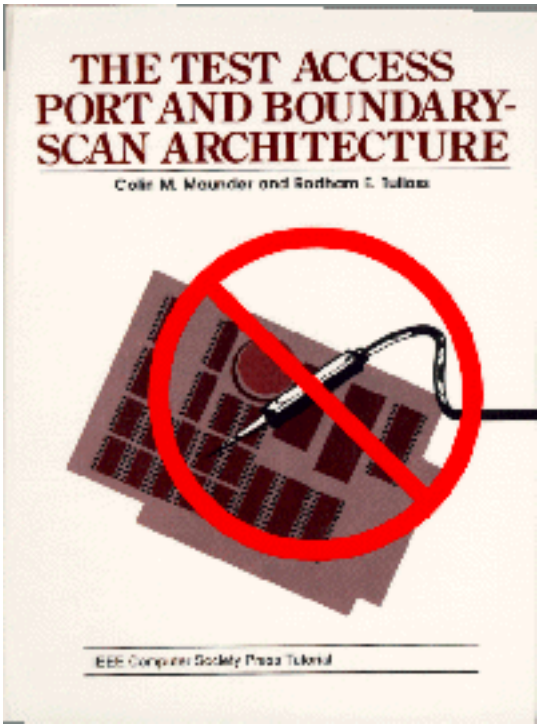
Since jtag-XLi is an at-speed solution, engineers can easily isolate and diagnose speed-related interconnect problems. These problems include defects related to common board-level problems such as cold solder joints, thin or narrow regions of interconnect, or thin insulation between levels of interconnect.

Momentum Data Systems, Inc. offers a dedicated 16-bit ISA (Industry Standard Architecture) AT-bus board MDS-TM1X-JTAG that can be significantly faster than a simple parallel port setup.

EST's visionICE family of scalable emulators is designed to span a full range of development needs and budgets. The system can be ordered as a low cost BDM/JTAG emulator, a networked BDM/JTAG emulator with Ethernet support, or as a full-featured in-circuit emulator delivering a high-end event, trace, and time stamp system.

EmuTec, based in Everett, Washington, is a leading supplier of Memory, JTAG and BDM emulators for test and development of embedded systems.

The Test Access Port and Boundary-Scan Architecture Colin M. Maunder and Rodham E. Tulloss (Eds), IEEE Computer Society Press, 1990



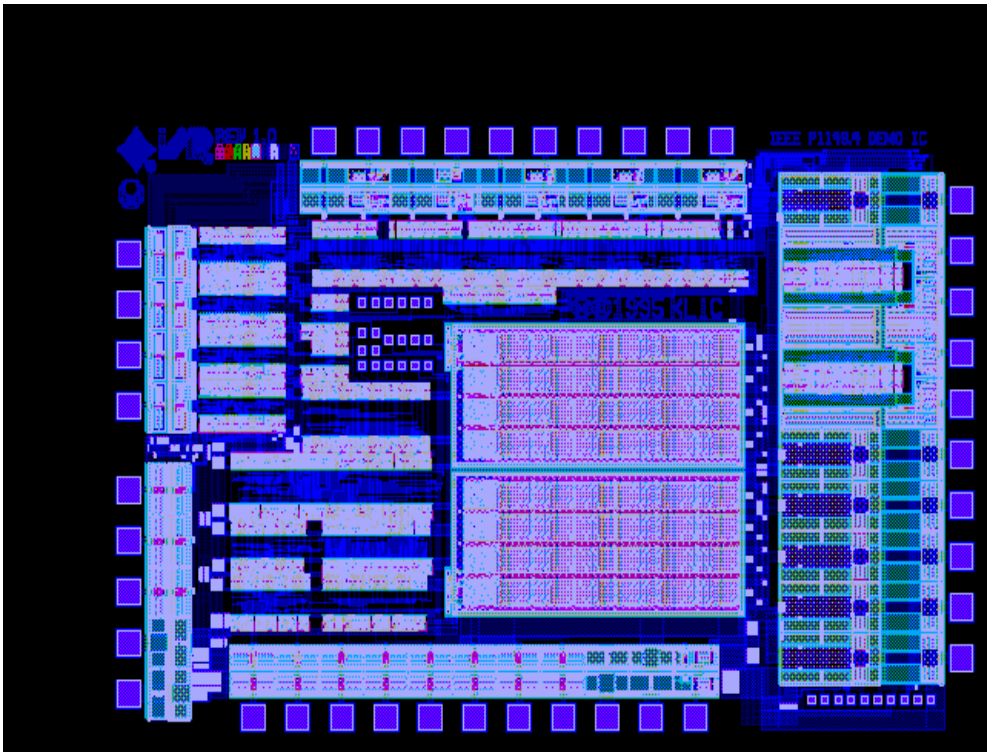
This book discusses the approaches to design-for-testability based on IEEE Standard 1149.1. The Test Access Port and Boundary-Scan Architecture explores the development of the standard, boundary-scan techniques, and solutions to the problems faced by this technology.

Alas, all is not rosy, there are pitfalls to JTAG. As with most good ideas, a bit of a land mine of intellectual property rights is involved. Texas Instruments patented its version, developed for the TMS320 DSP line, as U.S. Patent #5,329,471 titled "Emulation Devices, Systems and Methods Utilizing State Machines."

Obtaining IEEE Std 1149.1-1990

To learn more about IEEE Std 1149.1, please refer to the publications, IEEE Standard Test Access Port and Boundary-Scan Architecture, IEEE Std 1149.1-1990 (includes IEEE Std 1149.1a-1993) and Supplement to IEEE Std 1149.1-1990, IEEE Standard Test Access Port and Boundary-Scan Architecture, IEEE Std 1149.1b-1994. These documents are available through IEEE.

IEEE 1149.1 is a digital-only standard. Since many systems combine analog and digital, a new standard for mixed-signal testing is being developed, IEEE 1149.4. KLIC is working with the 1149.4 committee, and designed a test chip to test the new 1149.4 standard against real-world constraints.



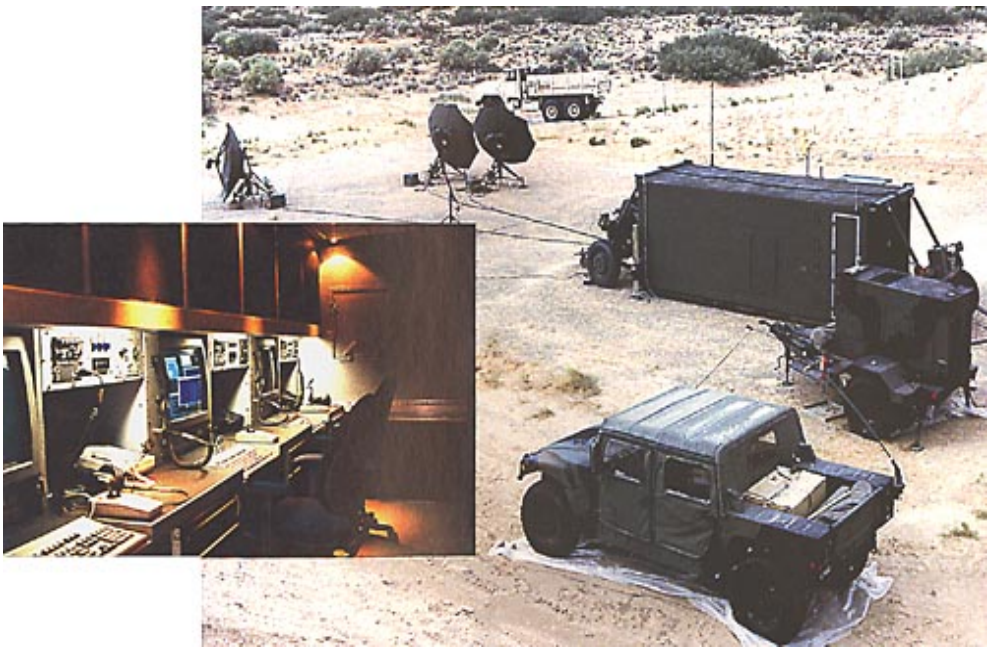
TEST CHIP for the IEEE 1149.4 Standard

A Standard for Testing of Electronic Mixed-Signal Systems without Nodal Access

The IEEE P1149.4 Mixed-Signal Test Bus Standard Working Group is defining, documenting, and promoting a standard mixed-signal test bus for use at the device and system levels to improve controllability and observability of mixed signal designs in order to reduce test development time and cost, and improve test quality.

Sometimes I'm amazed at what simple Internet searches can yield (like the Joint Tactical Ground Station (JTAGS)). JTAGS will receive and process data in-theater from space-based infrared sensors and disseminate warning, alerting and cueing information on Theater Ballistic Missiles and other tactical events of interest.

[If you don't think this fits here then you've never read *Circuit Cellar Neighborhood Strategic Defense Initiative Subtitle: The Ballistic Dynamics of Plastic Soda Bottles* by Steve Ciarcia & Ed Nisley; Circuit Cellar Issue: #2 Mar/Apr 1988.]



Characteristics: JTAGS is a theater tactical ground station contained in an 8 ft by 8 ft ISO shelter. The system is transportable by C-141aircraft and can be operational within hours. For redundancy, during contingency situations, the system will deploy in pairs. During crisis situations, the system will conduct joint operations. To reduce cost and accelerate fielding, JTAGS utilizes commercial off-the-shelf hardware with minor modifications to enhance transportability and deployment options. JTAGS is compatible with major existing communications systems and will interface with future planned communication systems.

If you would like to add any information on this topic or request a specific topic to be covered, contact Bob Paddock.
